REMARKS

The present Amendment amends claims 1, 6 and 11 and leaves claims 3, 5, 8 and 10 unchanged. Therefore, the present application has pending claims 1, 3, 5, 6, 8, 10 and 11.

Claims 1, 3, 5, 6, 8, 10 and 11 stand rejected under 35 USC §103(a) as being unpatentable over Fujimoto (U.S. Patent Application Publication No. 2002/0178336) in view of Banks (U.S. Patent No. 6,202,079) and Shimada (U.S. Patent Application Publication No. 2003/0221062). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1, 3, 5, 6, 8, 10 and 11 are not taught or suggested by Fujimoto, Banks or Shimada whether taken individually or in combination with each other as suggested by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Particularly, amendments were made to each of the independent claims to more clearly recite that the present invention is directed to a cache control method in a data processing system having a computer, which includes a synchronous point processing unit, for executing a program, and a storage unit having a cache memory for storing data transmitted as a result of execution of said program, a cache controller having a cache management table and a disk device having memory medium for storing data stored in said cache memory.

According to the present invention the synchronous point processing unit makes and sends a write request of updated data held in the memory

medium of data processed by the program in a write-through mode to update data of the program unreflected upon said disk device, issues a flush command to said storage unit in order to reflect the updated data upon the memory medium at a timing synchronous with a commitment to perform a transaction process, and makes and sends a write request, in the write-through mode, to said storage unit for requesting write of a synchronous point journal which records, in the storage unit, completion of a synchronous point process until a check point from said computer to said storage unit.

Further, according to the present invention the cache controller of the storage unit, responding to the flush command from the synchronous point processing unit, if a mode in said cache management table corresponding to a page for said flush command coincides with write-after, writes the page indicated by a cache pointer for the page in said cache management table to said memory medium and changes a cache management entry in said cache management table to a state of reflected. The cache controller of said storage unit, responding to said write request, if a mode designated during said write request is write-after, also writes data in said cache memory, and changes said cache management entry for the page to a state of unreflected, and responding to said write request, if said mode designated during said write request is not write-after, writes the page to both said cache memory and said memory medium, thereafter changes said cache management entry for the page to the state of reflected.

The above described features of the present invention as now more clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each

other. Particularly, the above described features of the present invention are as now more clearly recited in the claims are not taught or suggested by Fujimoto, Banks or Shimada whether taken individually or in combination with each other as suggested by the Examiner.

Fujimoto teaches, for example, a storage subsystem in which write data written in a first storage subsystem from a plurality of host computers each copied onto a second storage subsystem thereby protecting the write data in a multiplex manner. Fujimoto specifically teaches, for example, in paragraphs [0052] – [0054] that each disk subsystem includes a cache memory 11 and the cache memory is controlled by use of a cache management table 50 as illustrated, for example, in Figs. 2 and 3 thereof. Fujimoto teaches that the cache memory 11 temporarily stores data to be written to the disk array 12 through the disk adapter 12a. According to Fujimoto, a dirty flag 52 when set to "1" shows a state where the relevant write data is unreflected on the disk array 12 in the segments which holds the write data written in the cache memory by the host. As per Fujimoto, the master dirty flag 52 is set to "1" by the fibre channel target port 10a and the main frame system channel target port 10b at the time of writing the data and is reset to "0" by the disk adapter 12a after reflection on the disk array 12.

Thus, Fujimoto teaches operating the cache memory 11 according to write back processing rather than write through processing as in the present invention as recited in the claims. This is important since the considerations for maintaining data consistency are different between the write-back and write-through processings.

The present invention clearly recites that a synchronous point processing unit is provided so as to make and send a write request of updated data held in a memory of the program in a write through mode to update data of the program unreflected upon the disk device. Such a write through processing as recited in the claims is not taught or suggested by Fujimoto.

Further, there is no teaching or suggestion in Fujimoto of a synchronous point processing unit which performs various processings including sending a flush command as, for example, illustrated in Fig. 1 and Figs. 2 and 3 of the present application and writing of the synchronous point journal. There is no such teaching or suggestion in Fujimoto of the synchronous point processing unit as recited in the claims.

Thus, Fujimoto fails to teach or suggest a cache control method in a data processing system having a computer which includes a synchronous point processing section as recited in the claims.

Further, Fujimoto fails to teach or suggest that the synchronous point processing units makes and sends a write request of updated data held in a memory of data processed by the program in a write through mode to update data of the program unreflected upon the disk device, issues a flush command to the storage unit in order to reflect the updated data upon the memory at timing synchronous with the commitment to perform a transaction processing, and make and sends a write request in the write through mode, to the storage unit for requesting write of a synchronous point journal which records in the storage unit, completion of a synchronous point process until a check point from the computer to the storage unit as recited in the claims.

Therefore, as is quite clear from the above, Fujimoto fails to teach or suggest numerous features of the present invention now more clearly recited in the claims.

The above described deficiencies of Fujimoto are not supplied by any of the other references of record whether said references are taken individually or in combination with each other. Particularly, the above described features of the present invention shown above not to be taught or suggested by Fujimoto are also not taught or suggested by Banks and Shimada. Therefore, combining the teachings of Fujimoto with one or more of Banks and Shimada does not render obvious the features of the present invention as now more clearly recited in the claims.

Banks teaches a method for providing synchronization of a transaction in a data processing system where the transaction involves an initiator node, which starts the synchronization, and a coordinator node, which decides the outcome of the transaction. As taught by Banks, the initiator node and the coordinator node communicate through a routing node and synchronization is provided by establishing a first conversation between the initiator node and the routing node and a second conversation between the routing node and the coordinator node.

However, it is quite clear that Banks is not in anyway directed to the processing necessary to maintain consistency between cache memories in a storage system as in the present invention. Particularly, there is absolutely no teaching or suggestion in Banks of the timing necessary in the issuing of a flush command with respect to a cache memory and that the flush command is issued based on transactions of an application program operating on a host

relative to a storage system as in the present invention as recited in the claims.

Banks simply teaches, for example, in col. 2, lines 22-43 that a synchronous write occurs when state changes (checkpoints) are written to non-volatile storage synchronously with the transmission of messages during the two-phase commit protocol. This teaching of Banks is not in anyway related to the issuing of a flush command at a particular timing as in the present invention as now more clearly recited in the claims.

Thus, Banks fails to teach or suggest a cache control method in a data processing system having a computer which includes a synchronous point processing unit for executing a program and a storage unit having a cache memory for storing data transmitted as a result of execution of the program, a cache controller having a cache management table and a disk device having memory medium for storing data stored in the cache memory as recited in the claims.

Further, Banks fails to teach or suggest that the synchronous point processing unit makes and sends a write request of updated data held in the memory medium of data processed by the program in a write through mode to update data of the program reflected on the disk device, issues a flush command to the storage unit in order to reflect the updated data upon the memory medium at a timing synchronous with a commitment to perform a transaction process and makes and sends a write request, in the write through mode, to the storage unit for requesting write of a synchronous point journal which records, in the storage unit, completion of a synchronous point

process until a checkpoint from the computer to the storage unit as recited in the claims.

Shimada simply discloses a storage system having a cache memory which is operated according to the write back technique. Thus, Shimada teaches a system contrary to that of the present invention wherein the write through technique is used with respect to the cache memory.

Further, there is no teaching or suggestion in Shimada of the synchronous point processing unit and the operations performed by the synchronous point processing unit as recited in the claims. Thus, Shimada suffers from the same deficiencies relative to the features of the present invention as recited in the claims as both Fujimoto and Banks.

Therefore, since each of Fujimoto, Banks and Shimada each suffer from the same deficiencies relative to the features of the present invention as now more clearly recited in the claims, combining the teachings of Fujimoto, Banks and Shimada in the manner suggested by the Examiner in the Office Action does not render obvious the features of the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejection of claims 1, 3, 5, 6, 8, 10 and 11 as being unpatentable over Fujimoto in view of Banks and Shimada is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1, 3, 5, 6, 8, 10 and 11.

In view of the foregoing amendments and remarks, applicants submit that claims 1, 3, 5, 6, 8, 10 and 11 are in condition for allowance. Accordingly, early allowance of claims 1, 3, 5, 6, 8, 10 and 11 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.43870X00).

Respectfully submitted,

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